Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (canceled).

Claim 2 (canceled).

Claim 3 (canceled).

Claim 4 (canceled).

Claim 5 (canceled).

Claim 6 (canceled).

Claim 7 (canceled).

Claim 8 (canceled).

Claim 9 (currently amended): ~~A node controller for a node in a data storage system, the node being linked to another node and the nodes being locally coupled to a same host device and a same storage device, each node comprising one computer-memory complex and one node controller distinct from said one computer-memory complex, the~~ The node controller of claim 18, further comprising:

~~a memory controller for accessing a cluster memory of the node;~~

~~a plurality of logic engines each operable to perform a logic operation on non-address data originating from at least one data source in the data storage system and to write a result of the logic operation to a data destination in the data storage system, the logic engines performing the logic operation as instructed by a computer-memory complex of the node but without any further intervention by the computer-memory complex; and~~

command queues coupled to the logic ~~engines~~ engine, the command queues operable to store logic control blocks which can be processed by the logic ~~engines~~ engine.

Claim 10 (canceled).

Claim 11 (canceled).

Claim 12 (canceled).

Claim 13 (currently amended): The node controller of Claim [[9]] 18, wherein the node controller is implemented as an integrated circuit device.

Claim 14 (canceled).

Claim 15 (canceled).

Claim 16 (previously presented): The node controller of Claim 9, further comprising:

a producer register operable to specify a first address of a command queue; and

a consumer register operable to specify a second address of a command queue.

Claim 17 (canceled).

Claim 18 (currently amended) A node controller for a node in a data storage system having at least two nodes, each node comprising one computer-memory complex and one node controller distinct from said one computer-memory complex, the node controller comprising:

a memory controller ~~for coupling to~~ operable to interface the node controller with (1) a cluster memory that stores data being transferred through the node, and (2) ~~a backplane, wherein the backplane can be~~ a link coupled to ~~a plurality of other node controllers~~ another node controller in another node of the data storage system;

~~a plurality of~~ an input/output bus interface ~~interfaces for coupling~~ operable to interface the node controller with an input/output bus coupled to a computer-memory complex of the node [[,]] and at least one of a host device [[,]] and a storage device ~~all on a plurality of buses~~;

~~a plurality of logic engines~~ a logic engine coupled to (1) the memory controller, (2) the ~~backplane~~ link, and (3) the input/output ~~interfaces~~ bus interface;

wherein in a first type of data transfer, ~~one of the logic engines~~ the logic engine performs a logic operation to a plurality of data from one of a plurality of data sources in the data storage system and writes the result of the logic operation to one of a plurality of data destinations in the data storage system, the data sources comprising the cluster memory and the input/output

~~interfaces~~ bus interface, the data destinations comprising the cluster memory, the ~~backplane~~ link, and the input/output ~~interfaces~~ bus interface, the logic operation being used to calculate a parity data for writing a full or a partial RAID stripe or to reconstruct a lost data using the parity data.

Claim 19 (currently amended): The node controller of claim 18, wherein in a second type of data transfer, ~~one of the data sources~~ the input/output bus interface writes a data into the cluster memory and in response ~~one of the logic engines~~ the logic engine copies the data to ~~at least one of the data destinations~~ the another node via the link.

Claim 20 (canceled).

Claim 21 (currently amended): The node controller of claim 18, wherein ~~each of~~ the input/output bus interface ~~interfaces~~ comprises a peripheral component interconnect (PCI) ~~controller~~ control interface and ~~each of the buses~~ the input/output bus comprises a PCI bus.

Claim 22 (previously presented): The node controller of claim 21, wherein the computer-memory complex manages the PCI bus.

Claim 23 (previously presented): The node controller of claim 22, wherein the computer-memory complex supports a service selected from the group consisting of a HTTP service, a NFS service, and a CIFS service.

Claim 24 (previously presented): The node controller of claim 18, wherein the computer-memory complex is not burdened with temporarily storing data being transferred through the node in the computer-memory complex.

Claim 25 (previously presented): The node controller of claim 18, wherein the logic operation comprises an XOR operation.

Claim 26 (canceled).

Claim 27 (canceled).

Claim 28 (canceled).

Claim 29 (currently amended): A ~~node controller for a first~~ node in a data storage system comprising at least ~~the first node and a second node~~ two nodes, ~~each~~ the node comprising:

an input/output bus;

~~one~~ a computer-memory complex, comprising:

a central processing unit (CPU);

a system memory storing information for controlling data transfer through the node; and

a controller coupling the CPU, the system memory, and the input/output bus; and

~~one~~ a node controller distinct from ~~said one~~ the computer-memory complex, the node controller comprising:

a memory controller ~~for accessing~~ operable to interface the node controller with a cluster memory of the ~~first~~ node, the cluster memory storing data being transferred through the node;

~~one or more bus interfaces for communicating with~~ an input/output bus interface operable to interface the node controller with the input/output bus; ~~a host device, a data storage device, and a computer-memory complex of the first node all located on one or more buses;~~

a logic engine coupled to the memory controller, the input/output bus interface, and a link to ~~the second~~ another node of the data storage system;

wherein at least one of a host device and a storage device coupled to the input/output bus is able to read and write the cluster memory via the input/output bus, the logic engine is able to transfer data from the cluster memory to the another node via the link, and the memory controller is able to receive data from the another node via the link.

~~wherein in a first type of data transfer:~~

~~the computer-memory complex instructs the data storage device to write a data into the cluster memory;~~

~~the data storage device writes the data into the cluster memory via the one or more buses;~~

~~the computer memory complex instructs the node controller to send the data to the second node; and~~

~~the node controller sends the data to the second node via the link.~~

Claim 30 (canceled).

Claim 31 (canceled).

Claim 32 (canceled).

Claim 33 (canceled).

Claim 34 (canceled).

Claim 35 (new): The node of claim 29, wherein in a data transfer, the logic engine performs a logic operation on data from at least one of the input/output bus and the cluster memory, and writes a result of the logic operation to at least one of the input/output bus, the cluster memory, and the link.

Claim 36 (new): The node of claim 35, further comprising a command queue operable to store a logic control block to be processed by the logic engine, the logic control block specifying at least one data source and at least one data destination for the logic operation.

Claim 37 (new): The node of claim 36, further comprising:

a producer register operable to specify a first address of the command queue; and

a consumer register operable to specify a second address of the command queue.

Claim 38 (new): The node of claim 35, wherein the logic engine comprises an exclusive OR (XOR) engine.

Claim 39 (new): The node of claim 38, wherein the XOR engine is used to calculate a parity data for writing a full or a partial RAID stripe.

Claim 40 (new): The node of claim 38, wherein the XOR engine is used to reconstruct a lost data using a parity data.

Claim 41 (new): The node of claim 29, wherein the node controller is implemented as an integrated circuit device.

Claim 42 (new): The node of claim 29, wherein the input/output bus interface comprises a peripheral component interconnect (PCI) control interface and the input/output bus comprises a PCI bus.

Claim 43 (new): The node of claim 29, wherein the node controller is operable to be programmed by the computer-memory complex.

Claim 44 (new): The node of claim 29, wherein in a data transfer, the input/output bus interface writes a data into the cluster memory and in response the logic engine copies the data to the another node via the link.

Claim 45 (new): The node of claim 29, wherein the computer-memory complex supports a service selected from the group consisting of a HTTP service, a NFS service, and a CIFS service.

Claim 46 (new): The node of claim 29, wherein the computer-memory complex is not burdened with temporarily storing data being transferred through the node in the system memory.

Claim 47 (new): The node of claim 29, further comprising:

> another input/output bus interface operable to interface the node controller with another input/output bus coupled to the computer-memory complex and at least one of another host device and another storage device, wherein the computer-memory complex, the another host device, and the another storage device are able to read and write the cluster memory via the another input/output bus.

Claim 48 (new): A node in a data storage system having at least one node for providing access to a data storage facility, the node comprising a node controller and a computer memory complex, the node controller distinct from the computer-memory complex, the node controller comprising:

> an input/output bus interface operable to interface the node controller with an input/output bus that is coupled to the computer-memory complex and that is couplable to at least one of a host device and a storage device;

a memory controller operable to interface the node controller with a cache memory in the node;

one or more logic engines coupled to the input/output bus interface, to the memory controller, and to a link that can be coupled to another node in the data storage system;

wherein the node controller is arranged so that the computer-memory complex, the host device, and the storage device are able to access the node controller via the input/output bus so that the host device and the storage device are able to read and write the cache memory via the input/output bus; and

wherein the logic engine is able to transfer data from the cache memory to another node in the data storage system via the link, and the memory controller is able to receive data from the another node in the data storage system via the link.

Claim 49 (new): The node of claim 48, wherein the logic engine is operable to perform a logic operation in a data transfer on data from at least one of the input/output bus and the cluster memory, and to write a result of the logic operation to at least one of the input/output bus, the cluster memory and the link.

Claim 50 (new): The node of claim 49, wherein the logic engine comprises an exclusive OR engine.

Claim 51 (new): The node of claim 49, the node controller further comprising a command queue operable to store a logic control block to be processed by the logic engine, the logic control block specifying a data source and data destination for the logic operation.

Claim 52 (new): The node of claim 48, wherein the node controller is implemented as an integrated circuit device.

Claim 53 (new): The node of claim 48, wherein the input/output bus interface comprises a peripheral component interconnect control interface and the input/output bus comprises a peripheral component interconnect bus.

Claim 54 (new): The node of claim 48, wherein the node controller is operable to be programmed by the computer-memory complex.

Claim 55 (new): The node of claim 51, the node controller further comprising:

a producer register operable to specify a first address of the command queue; and

a consumer register operable to specify a second address of the command queue.

Claim 56 (new): The node of claim 48, wherein the node controller is arranged to send data written into the cache memory to the another node via the link.

Claim 57 (new): The node of claim 48, wherein the computer-memory complex is arranged to support a service selected from the group consisting of a HTTP service, a NFS service, and a CIFS service.

Claim 58 (new): The node of claim 48, wherein the computer-memory complex is not burdened with temporarily storing data being transferred through the node in the computer-memory complex.

Claim 59 (new): The node of claim 50, wherein the exclusive OR engine is arranged to calculate a parity data for writing a full or a partial RAID stripe.

Claim 60 (new): The node of claim 50, wherein the exclusive OR engine is arranged to reconstruct lost data using a parity data.

Claim 61 (new): The node of claim 48, wherein the node controller is configured to act as a slave device.